DETAILED ACTION

1. The amendment filed 08/16/2007 has been received and considered.

Claims 1-12 and 16-20 are presented for examination.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Michael R. Hardaway (Registration # 52992 at Patterson & Sheridan, LLP) on 22nd October 2007 at 4:10 pm.

3. The application has been amended as follow:

DEO 12/3/07

Claim 1 line 2 the word "target" has been replaced with the phrase --hardware target--.

Claim 13-15 has been canceled.

Claim 11 has been replaced with the following:

-- 11. A method of processing signals wit a modified netlist within a software-based logic simulation tool comprising the step of:

creating a netlist of objects specifying each object for a target hardware architecture, wherein the target hardware architecture is a field programmable gate array;

identifying objects specific to the target hardware architecture that are repeated to identify potential dummy object;

creating a list objects, from the netlist of objects, that are used by a circuit design to be implemented in the target hardware architecture;

forming a list of unused objects in the target hardware architecture from the netlist of objects and the list of objects used by the circuit design;